ST. ANNE'S COLLEGE OF ENGINEERING AND TECHNOLOGY

ANGUCHETTYPALAYAM, PANRUTI-607 110

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Lab Manual

EC8462 – LINEAR INTEGRATED CIRCUITS LABORATORY

EC8462 LINEAR INTEGRATED CIRCUITS LABORATORY

LIST OF EXPERIMENTS:

DESIGN AND TESTING OF

1. Inverting, Non inverting and Differential amplifiers.
2. Integrator and Differentiator.
3. Instrumentation amplifier
4. Active low-pass, High-pass and band-pass filters.
5. Astable & Monostable multivibrators and Schmitt Trigger using op-amp.
6. Phase shift and Wien bridge oscillators using op-amp.
7. Astable and monostable multivibrators using NE555 Timer.
8. PLL characteristics and its use as Frequency Multiplier.
9. R-2R Ladder Type D - A Converter using Op amp.
10. DC power supply using LM317 and LM723.
11. Study of SMPS.

SIMULATION USING SPICE

1. Active low-pass, High-pass and band-pass filters using Opamp
2. Astable and Monostable multivibrators using NE555 Timer
3. A/D converters
4. Analog multiplier

1. INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS.

1(a) INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

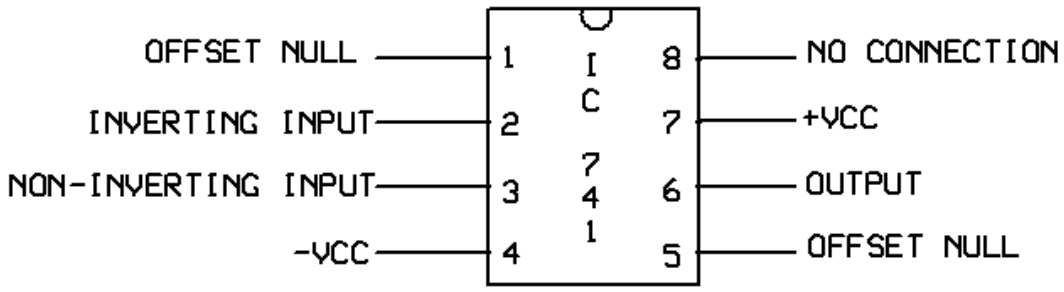
$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

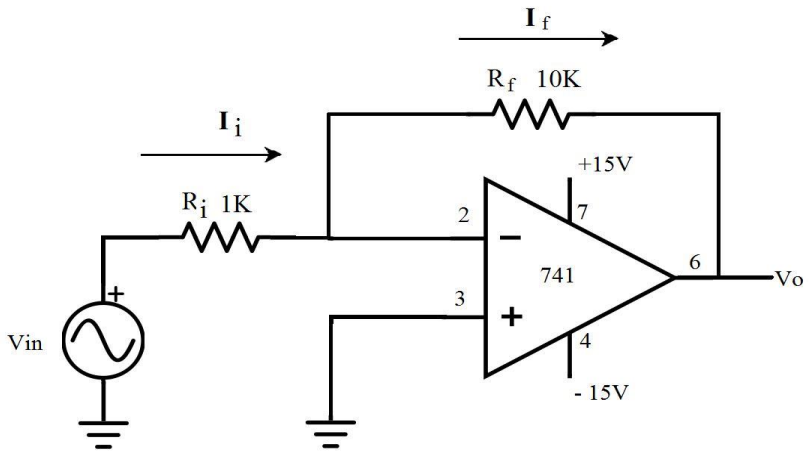
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

Gain of an inverting amplifier $Av = V_o/V_{in} = -R_f / R_i$

The required gain = 10,

That is $Av = -R_f/R_i = 10$

Let $R_i = 1K\Omega$, Then $R_f = 10K\Omega$

Observations:

Vin = 1 Vpp

Vo=?

Gain, Av = Vo/Vin =?

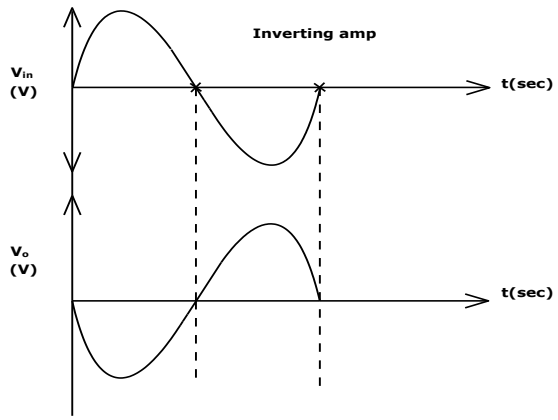
Observed phase difference between the input and the output on the CRO =?

Calculation:

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

MODEL GRAPH:



RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn**.**

VIVA QUESTIONS:

1. What is an op-amp?
2. What is an inverting amplifier?
3. What is the difference between inverting and non inverting amplifier?
4. Define CMRR.
5. Write the equation for gain of an inverting amplifier.

1(b) NON - INVERTING AMPLIFIER

AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$V_o = A_{CL} V_i$$

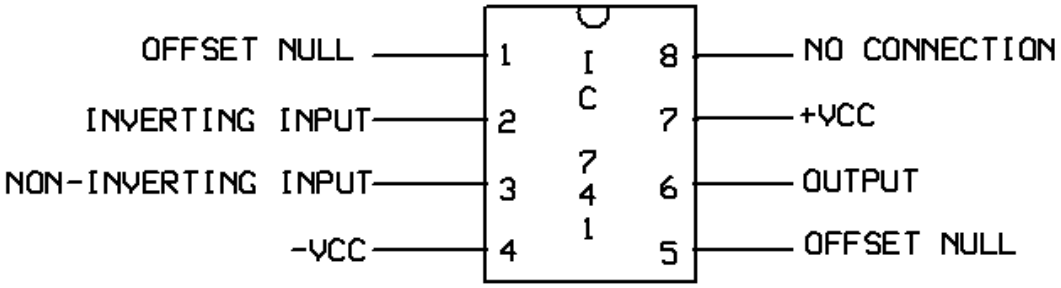
Here the output voltage is in phase with the input signal.

PROCEDURE:

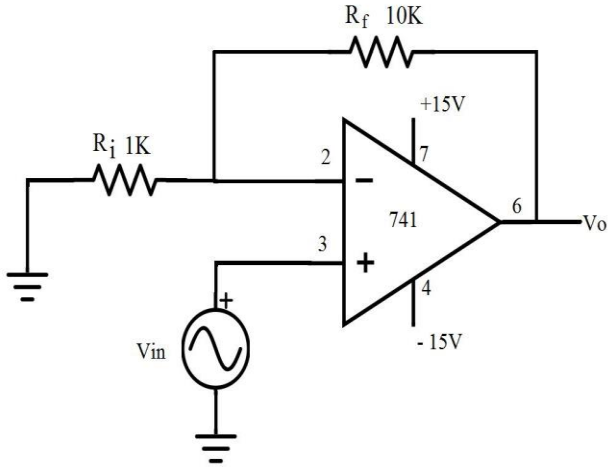
1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.

4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



DESIGN:

Gain of an inverting amplifier $Av=V_o/V_{in} = 1+R_f/ R_i$,

Let the required gain be 11,

Therefore $Av= 1+R_f/ R_i= 11$

$R_f/ R_i = 10$

Take $R_i= 1K\Omega$, Then $R_f = 10K\Omega$

Vin = 1Vpp

Vo = ?

Gain Av = Vo/Vin =?

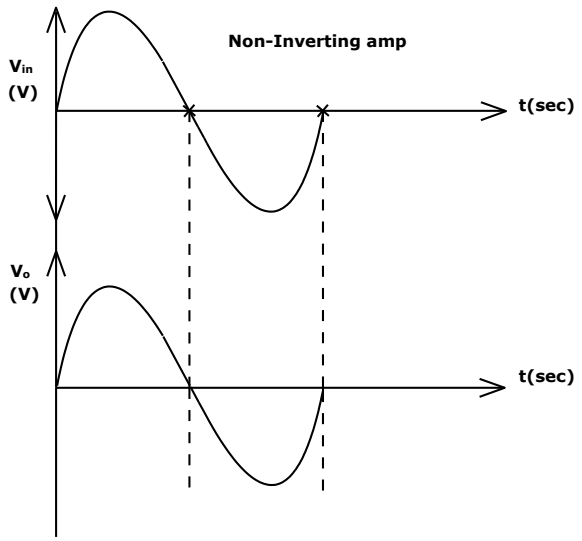
Observed phase difference between the input and the output on the CRO =?

CALCULATION:

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

MODEL GRAPH:



RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn.

VIVA QUESTIONS:

1. What is an op-amp?
2. What is an non- inverting amplifier?
3. What is the difference between inverting and non inverting amplifier?
4. Define CMRR.
5. Write the equation for gain of an non- inverting amplifier.

1(C) DIFFERENTIAL AMPLIFIER

AIM:

To design a differential Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

Differential Z_{in} (between the two input pins) = $R_1 + R_2$ (Note: this is approximate)

For common-mode rejection, anything done to one input must be done to the other. The addition of a compensation capacitor in parallel with Rf, for instance, must be balanced by an equivalent capacitor in parallel with Rg.

Whenever $R_1 = R_2$and $R_f = R_g$, the differential gain is

$$V_{out} = A(V_2 - V_1) \text{ and } A \triangleq \frac{R_f}{R_1}$$

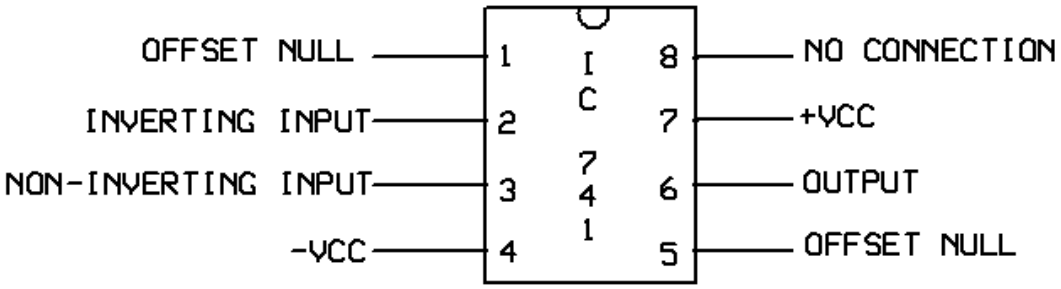
When $R_1 = R_f$and $R_2 = R_g$the differential gain is A = 1 and the circuit acts as a differential follower:

$$V_{out} = V_2 - V_1$$

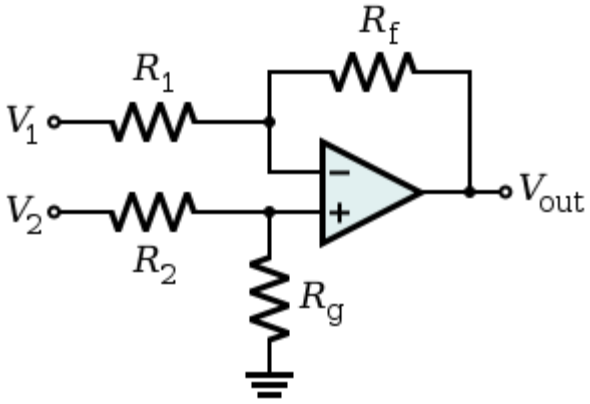
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIAL AMPLIFIER:



DESIGN:

$$V_{\text{out}} = \frac{(R_\text{f} + R_1)\,R_\text{g}}{(R_\text{g} + R_2)\,R_1} V_2 - \frac{R_\text{f}}{R_1} V_1$$

Differential Z_{in} (between the two input pins) = R_1 + R_2 (Note: this is approximate)

For common-mode rejection, anything done to one input must be done to the other. The addition of a compensation capacitor in parallel with Rf, for instance, must be balanced by an equivalent capacitor in parallel with Rg.

Whenever $R_1 = R_2$and $R_\text{f} = R_\text{g}$, the differential gain is

$$V_{\text{out}} = A(V_2 - V_1) \text{ and } A \triangleq \frac{R_f}{R_1}$$

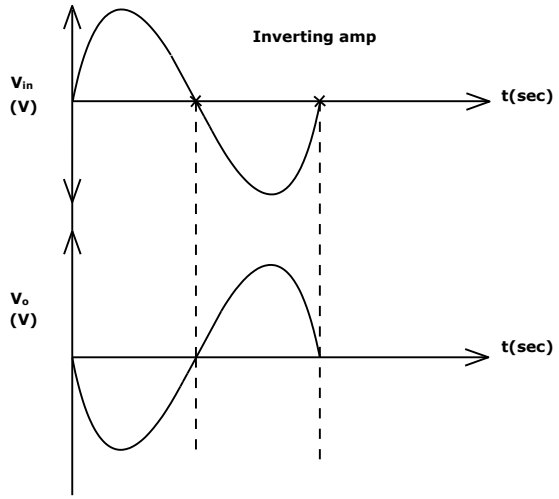
When $R_1 = R_f$ and $R_2 = R_g$ the differential gain is A = 1 and the circuit acts as a differential follower:

$$V_{\text{out}} = V_2 - V_1$$

OBSERVATIONS:

S.No		Input	Output
1.	Amplitude in differential mode (No. of div x Volts per div)		
2	Amplitude in common mode (No. of div x Volts per div)		
3	Time period (No. of div x Time per div)		

MODEL GRAPH:



RESULT:

The design and testing of the differential amplifier is done and the input and output waveforms were drawn.

2.INTEGRATOR AND DIFFERENTIATOR.

2(a) INTEGRATOR:

AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

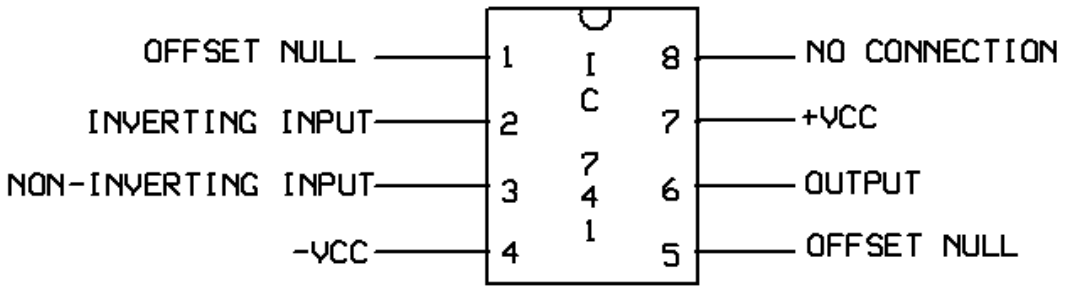
A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

$$V_o = - (1/R_f C_1) \int V_i \, dt$$

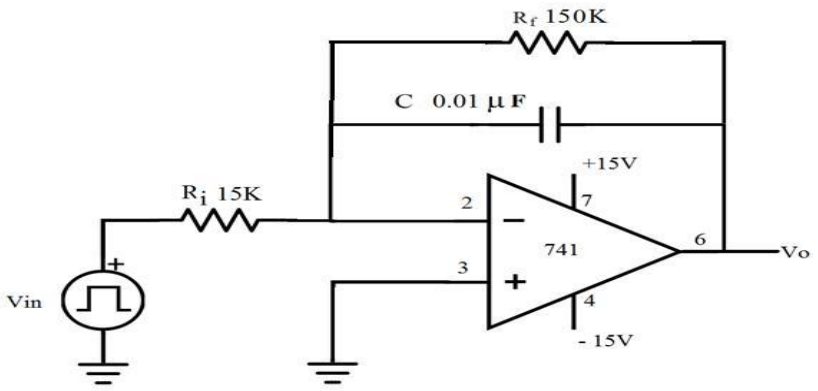
Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is, $T \geq R_f C_f$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



DESIGN:

Given f =1 KHz

So T = 1/f = 1ms

Design equation is $T = 2\pi R_i C$

Let $C = 0.01\mu F$

Then $R_i = 15K\Omega$

Take $R_f = 10R_i = 150K\Omega$

[To obtain the output of an Integrator circuit with component values $R_1C_f = 0.1ms$, $R_f = 10\ R_1$ and $C_f = 0.01\ \mu F$ and also if 1 V peak square wave at 1000Hz is applied as input.]

We know the frequency at which the gain is 0 dB, $f_b = 1 / (2\pi\ R_1\ C_f)$
Therefore f_b = _____
Since $f_b = 10\ f_a$, and also the gain limiting frequency $f_a = 1 / (2\pi\ R_f\ C_f)$
We get , R_1 = _____ and hence R_f = _____

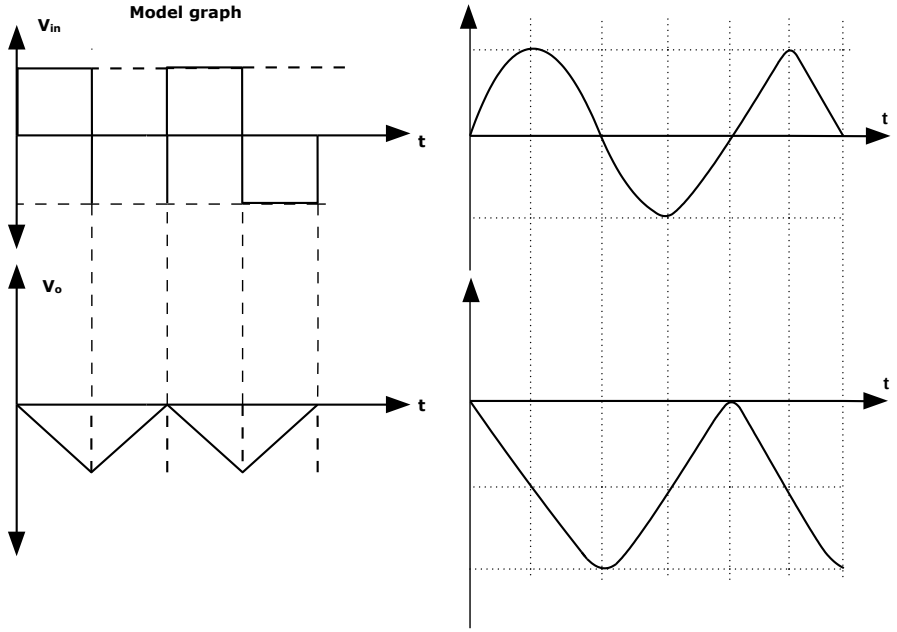
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

MODEL GRAPH:



CALCULATION:

RESULT:

The design of the Integrator circuit was done and the input and output waveforms were obtained**.**

2(b) DIFFERENTIATOR

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 . The expression for the output voltage is given as,

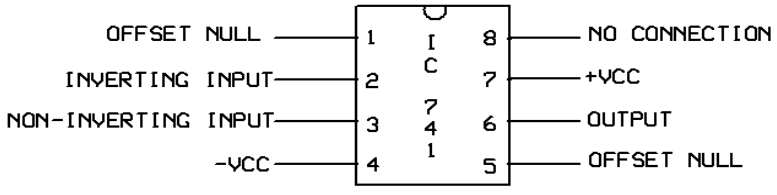
$$V_o = - R_f C_1 (dV_i /dt)$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

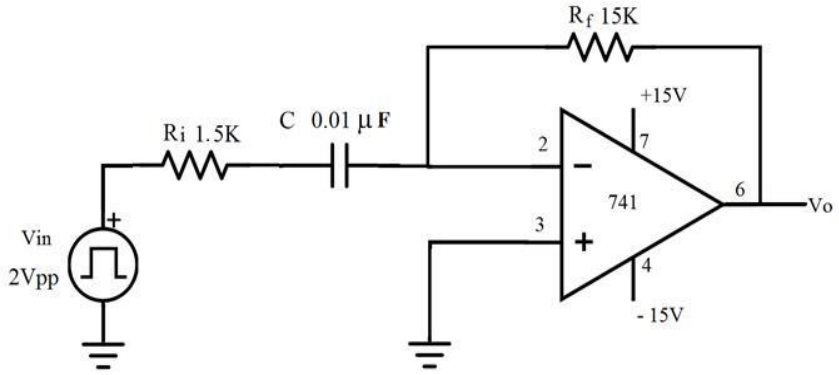
1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ µF, calculate the value of R_f.
2. Choose $f_b = 20 f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIATOR:



DESIGN :

Given f = 1 KHz

So T = 1/f = 1ms

Design equation is $T = 2\pi R_f C$

Let C = 0.01µF

Then R_f = 15KΩ

Let Ri = Rf/10 = 1.5KΩ

[To design a differentiator circuit to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator , draw its output waveform.]

Given f_a = 1 KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$

Let us assume C_1 = 0.1 µF; then

R_f = _____

Since $f_b = 20 f_a$, f_b = 20 KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence R_1 = _____

Also since $R_1C_1 = R_f C_f$; Cf = _____

Given V_p = 1 V and f = 1000 Hz, the input voltage is $V_i = V_p \sin \omega t$

We know $\omega = 2\pi f$

Hence

$V_o = - R_f C_1 (dV_i/dt)$

$= - 0.94 \cos \omega t$

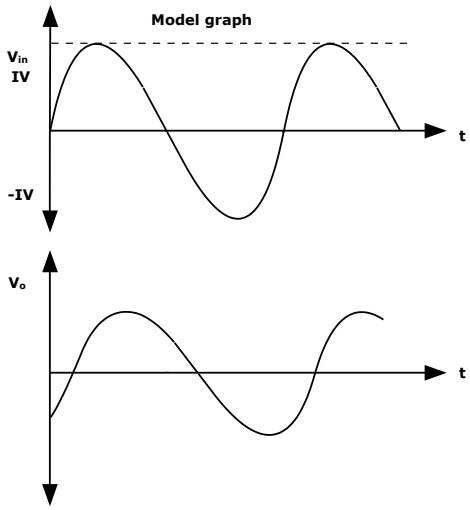
PROCEDURE:

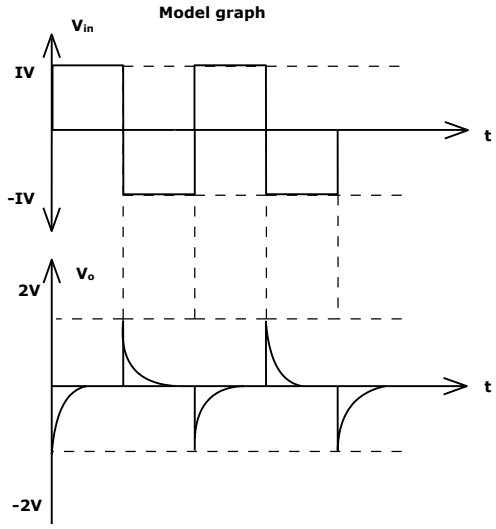
1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No		amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

MODEL GRAPH:





CALCULATION:

RESULT:

The design of the Differentiator circuit was done and the input and output waveforms were obtained.

VIVA QUESTIONS.

1. Define an integrator.
2. State the applications of an integrator.
3. What is a differentiator?
4. What are the steps to design a differentiator?
5. What are the steps to design an integrator?

3. INSTRUMENTATION AMPLIFIER.

AIM:

To design a instrumentation Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

An **instrumentation** (or **instrumentational**) **amplifier** is a type of differential amplifier that has been outfitted with input buffers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short- and long-term are required.

The most commonly used instrumentation amplifier circuit is shown in the figure. The gain of the circuit is

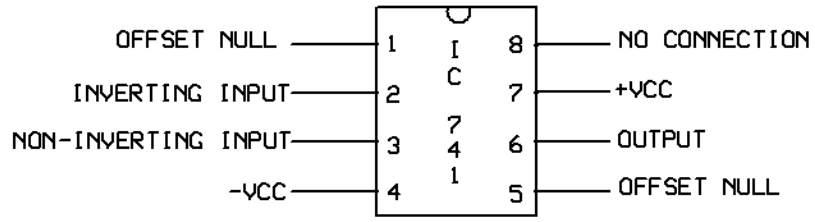
$$\frac{V_{\text{out}}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{\text{gain}}}\right)\frac{R_3}{R_2}$$

The rightmost amplifier, along with the resistors labelled R_2 and R_3 is just the standard differential amplifier circuit, with gain = R_3 / R_2 and differential input resistance = $2 \cdot R_2$. The two amplifiers on the left are the buffers. With R_{gain} removed (open circuited), they are simple unity gain buffers; the circuit will work in that state, with gain simply equal to R_3 / R_2 and high input impedance because of the buffers. The buffer gain could be increased by putting resistors between the buffer inverting inputs and ground to shunt away some of the negative feedback; however, the single resistor R_{gain} between the two inverting inputs is a much more elegant method: it increases the differential-mode gain of the buffer pair while leaving the common-mode gain equal to 1.

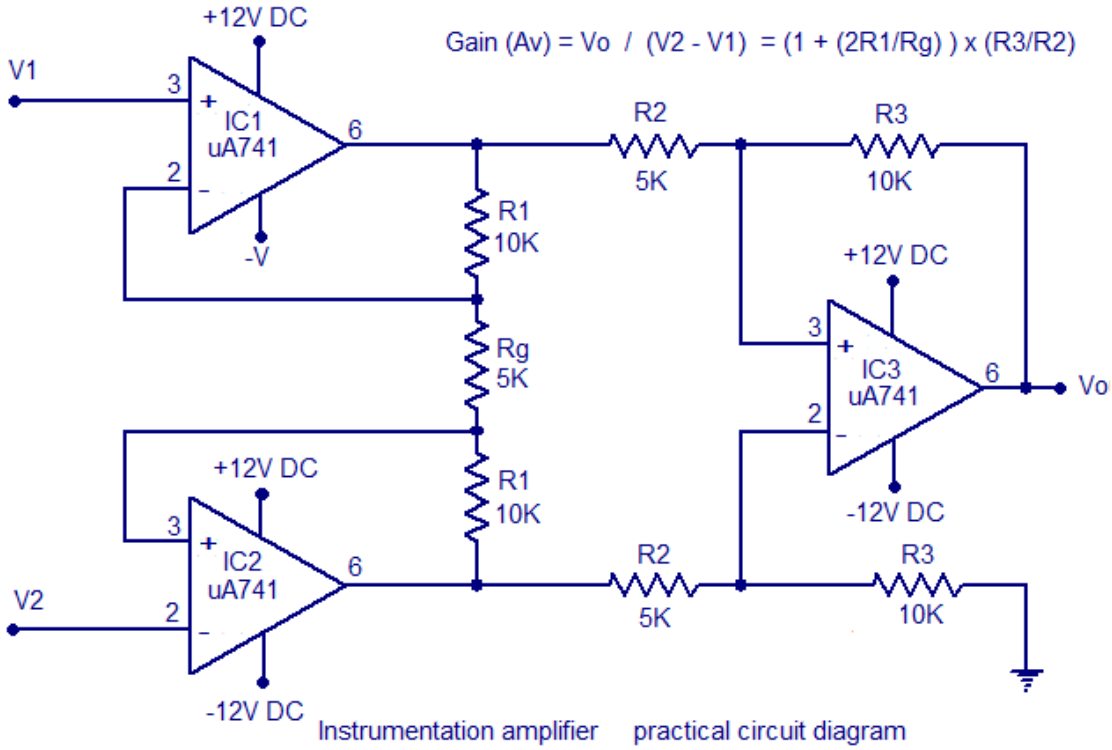
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INSTRUMENTATION AMPLIFIER:



OBSERVATIONS:

S.No		Amplitude	Time period
1.	Input		
2	Output		

RESULT:

The design and testing of the instrumentation amplifier is done and the input and output waveforms were drawn.

VIVA QUESTIONS:

1. What are the features of instrumentation amplifier?
2. What are the applications of instrumentation amplifier?
3. What is an instrumentation amplifier?
4. Write the expression for output voltage.
5. What is the use of transducer in an instrumentation amplifier?

4. ACTIVE LOWPASS, HIGHPASS AND BANDPASS FILTERS

Aim:-

To design and test the frequency response of a second order LPF, HPF and BPF.

Components Required:-

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Resistors		
3.	Capacitor	O.01μf , O.05μf	2 each
4.	CRO		1
5.	Power Supply	± 15V	1
6.	Probe		2
7.	Bread Board		1

Theory:-

LPF:-

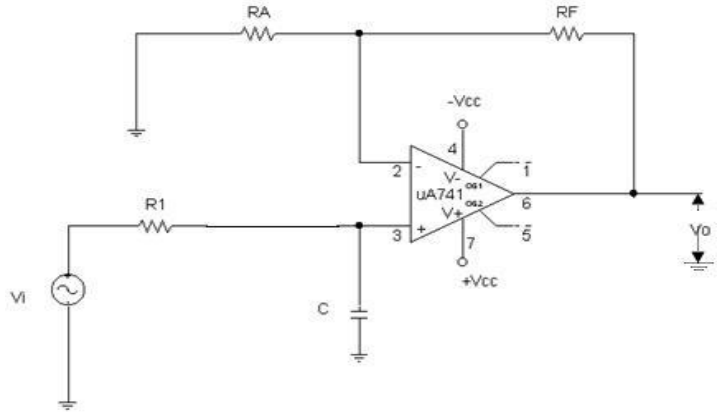
A LPF allows only low frequency signals up to a certain break-point f_H to pass through, while suppressing high frequency components. The range of frequency from 0 to higher cut off frequency f_H is called pass band and the range of frequencies beyond f_H is called stop band.

The following steps are used for the design of active LPF.

1. The value of high cut off frequency f_H is chosen.
2. The value of capacitor C is selected such that its value is $\leq 1\mu F$.
3. By knowing the values of f_H and C, the value of R can be calculated using
$$f_H = \frac{1}{2\pi RC}$$
4. Finally the values of R_1 and R_f are selected depending on the designed pass band gain by using $A = 1 + \left(\frac{R_f}{R_1}\right)$

Circuit Diagram:-

Second Order LPF:



Design:-

Second order:-

Given frequency, f_H = 2 KHz and gain =2

Let C=0.01μf

The frequency, $f_H = \dfrac{1}{2\pi\sqrt{\left(2\times10^{3}\right)\left(0.01\times10^{-6}\right)}}$

Set, $R_2 = R_3 = R$

$C_2 = C_3 = C$

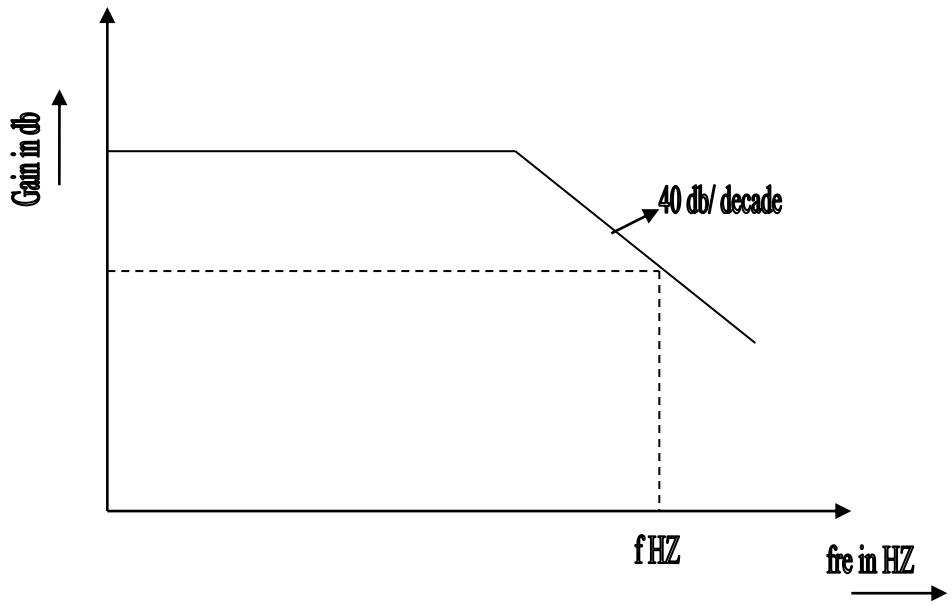
$\therefore f_H = \dfrac{1}{2\pi RC}$

Tabulation

Second order LPF Vin=1V

S.No	Frequency (Hz)	O/p voltage(v)	Gain=Vo/Vin	Gain=20log(Vo/Vin)

Model graph:-

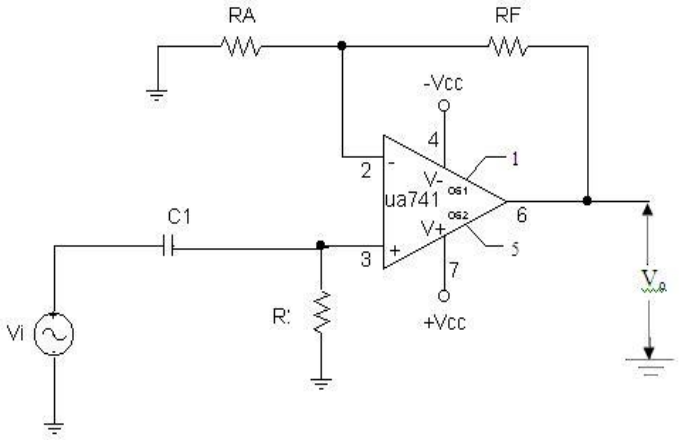


Second order HPF:

Theory:-

The high pass filter is the complement of the low pass filter. Thus the high pass filter can be obtained by interchanging R and C in the circuit of low pass configuration. A high pass filter allows only frequencies above a certain bread point to pass through and at terminates the low frequency components. The range of frequencies beyond its lower cut off frequency f_L is called stop band.

Circuit Diagram:-
Second Order HPF:



Design:-

$$f_L = 2KHZ$$

$$C = 0.01\mu F$$

$$Gain,\ Av = 2$$

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$Let\ \ R_2 = R_3 = R$$
$$C_2 = C_3 = C$$

$$R_2 = R_3 = \frac{1}{2\pi f L C}$$

$$R_2 = R_3 = 7.95k\Omega$$

$$A = 1 + \frac{R_f}{R_1} = 2$$

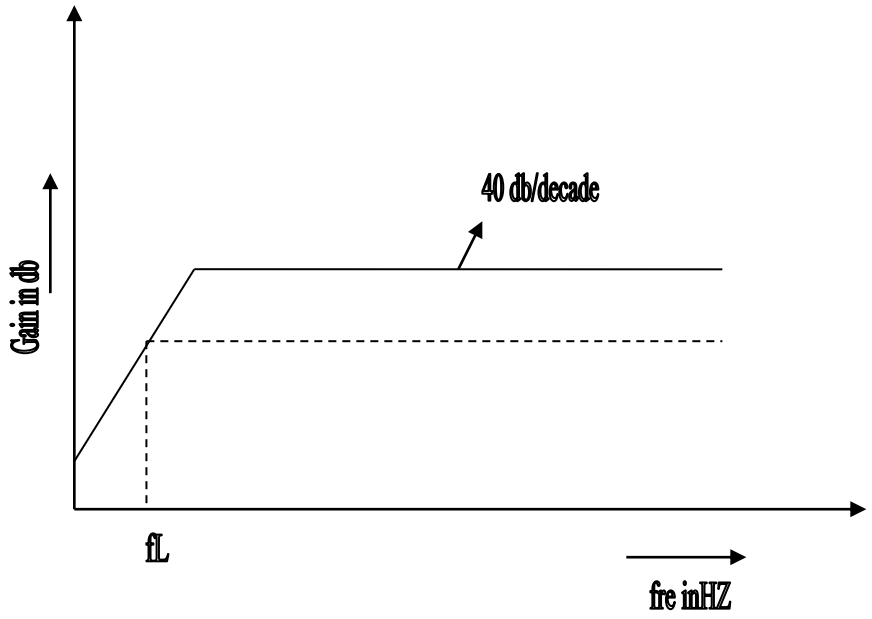
$$\therefore R_f = R_1 = 10k\Omega(given)$$

Observation:

Vin=1V

S.No	Frequency (Hz)	O/p voltage(v)	Gain=Vo/Vin	Gain=20log(Vo/Vin)

Model graph:-



Procedure:-

LPF:-

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

HPF

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.

4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

Theory:-

BPF:-

The BPF is the combination of high and low pass filters and this allows a specified range of frequencies to pass through. It has two stop bands in range of frequencies between 0 to f_L and beyond f_H. The band b/w f_L and f_H is called pass band. Hence its bandwidth is (f_L-f_H). This filter has a maximum gain at the resonant frequency (f_r) which is defined as

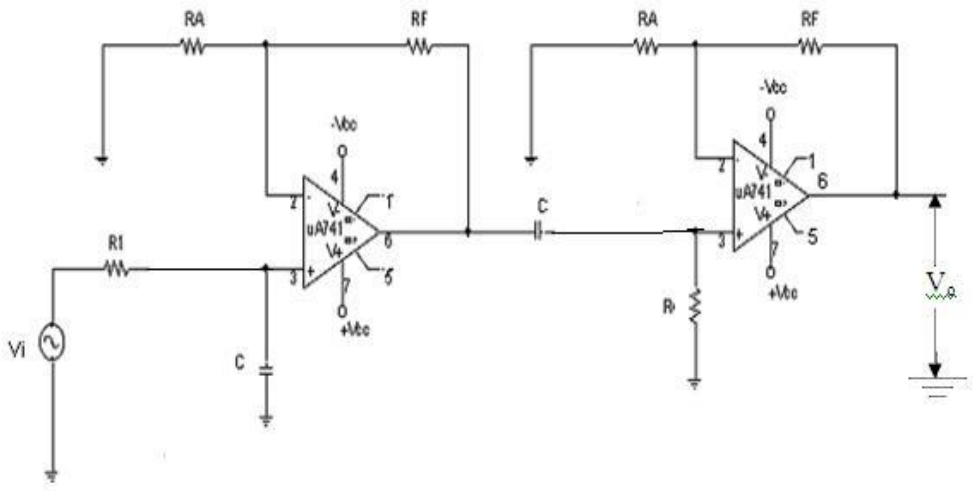
$$f_r = \sqrt{f_H f_L}$$

The figure of merit (or) quality factor Q is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{BW}$$

Circuit Diagram:-

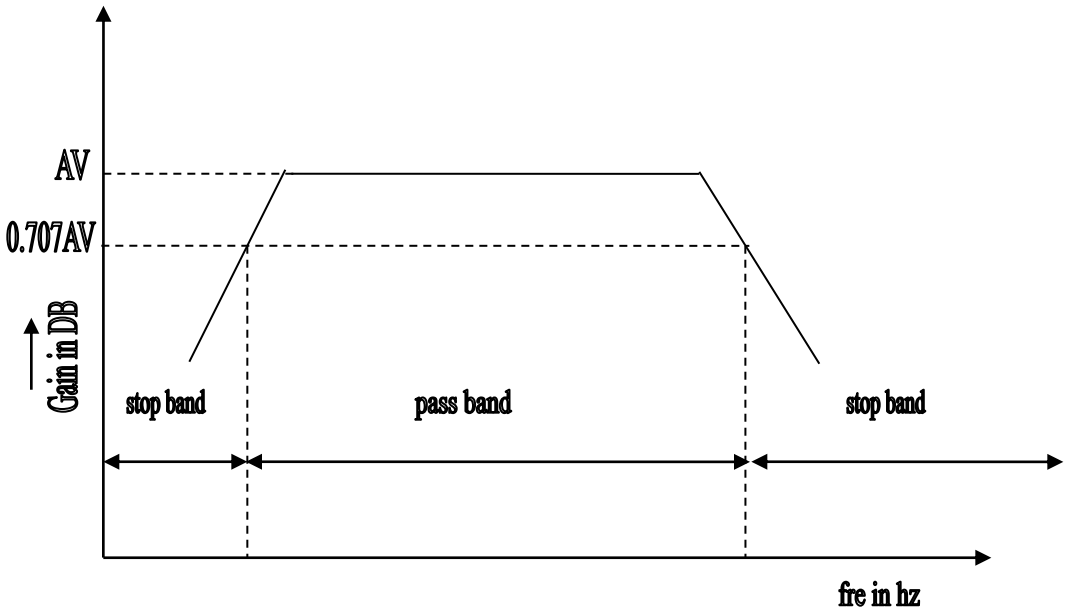
BPF



Low Pass Filter High Pass Filter

Model graph:-

BPF:-



Tabulation:-

BPF Vin=50mv

S.No	Frequency (Hz)	Vo(volts)	Gain=20log(Vo/Vin)

Procedure:

BPF:-

1. The input signal is connected to the circuit from the signal generator.
2. The input and output signals are connected to the filter.
3. The suitable voltage is selected.
4. The correct polarity is checked.
5. The steps are repeated.

Result:-

Thus the frequency response of second order LPF,HPF and BSF filter was designed and tested.

5. ASTABLE AND MONOSTABLE MULTIVIBRATORS AND SCHMITT TRIGGER USING OP-AMP

Aim:

To design and test an astable and monostable multivibrators and schmitt trigger using op-amp

Apparatus Required:

S.No	Component	Range	Quantity
1.	Op amp	IC 741	1
2.	DTS	(0-30) V	1
3.	CRO		1
4.	Resistor		1
5.	Capacitors	–	–
6.	Diode	IN4001	2
7.	Probes	–	1

Design:

1. Monostable Multivibrators:

$\beta = R_2/R_1+R_2$ [$\beta = 0.5$ & $R_1 = 10$ K]

Find R_2 = ; R3 = 1K; R4 = 10K;

Let F =_____KHz ; C= 1mfd; C4 = 0.1mfd

Pulse width, T = 0.69RC

Find R =

Time Period T= 0.69RC

Let T = 1ms; and C = 0.1μF.

Then R = 15KΩ

Feedback factor $\beta = R_2/(R_1+R_2)$

Let $\beta = 0.5$ or 1/2

$R_2/(R_1+R_2) = 1/2$

If R_1=10KΩ ; R_2 =10KΩ

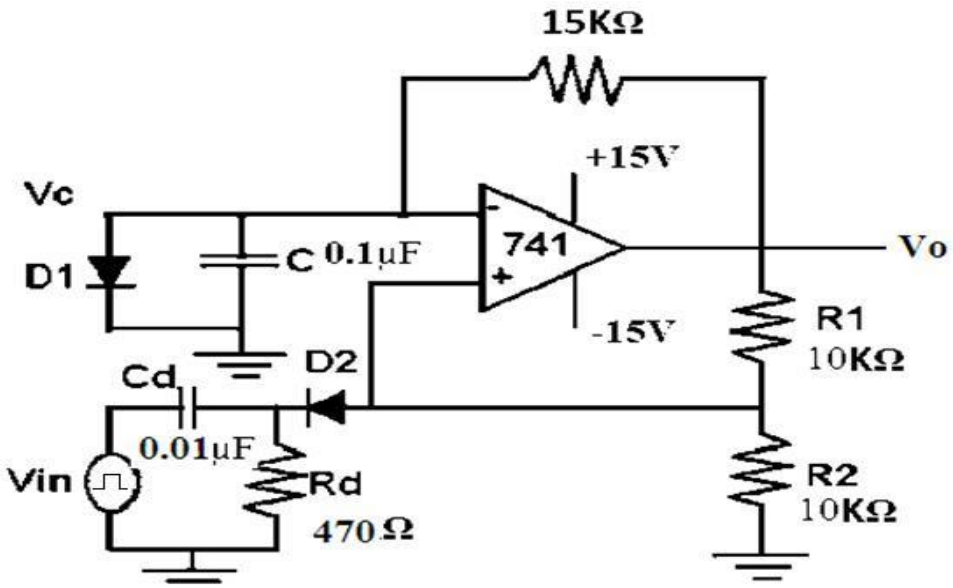
For triggering circuit

R_dC_d= 0.0016t

Let t = 3ms and C_d = 0.01 μF; then Rd = 470Ω

D_1 & D_2 are diodes 1N 4001

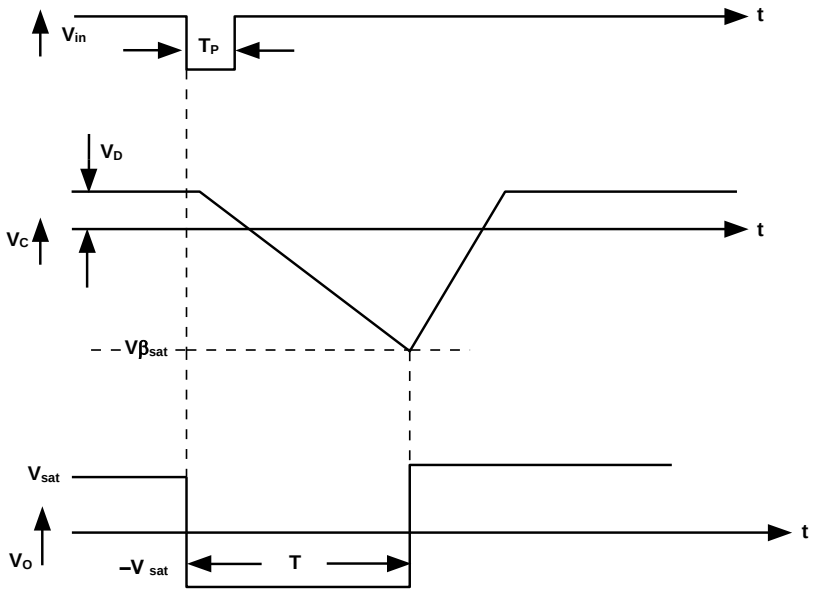
Circuit Diagram



Tabulation:

S.No		amplitude	Time period	
			Ton	Toff

Model graph:



Procedure:

1. Make the connections as shown in circuit diagram.
2. A trigger pulse is given through differentiator circuit through pin no.3
3. Observe the pulse waveform at pin no.6 using CRO and note down the time period.
4. Plot the waveform on the graph.

2. Astable Multivibrators:

Design: T = 2RC

$R_1 = 1.16\ R_2$

Given f_O = _____KHz

Frequency of Oscillation fo = 1 / 2 RC if $R_1 = 1.16R_2$

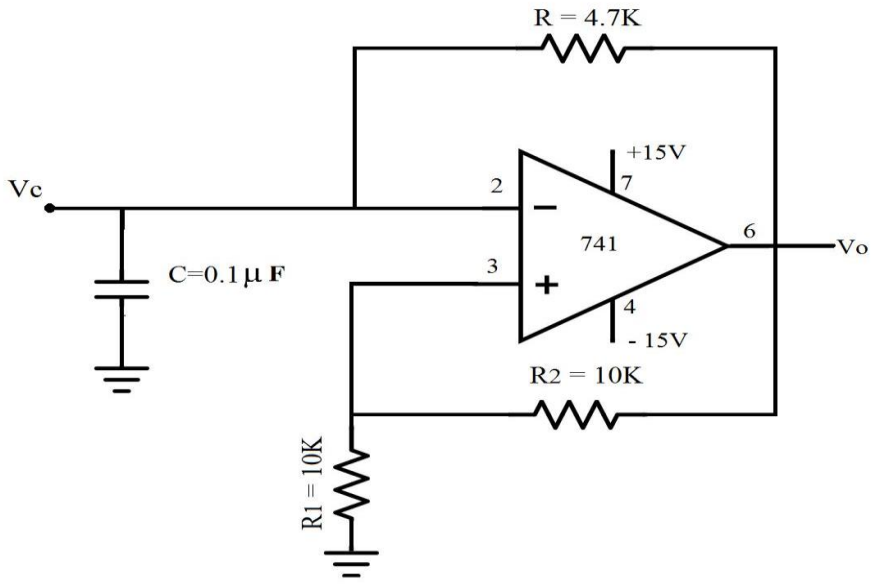
Let R_2 = 10 KΩ

$R_1 = 10 * 1.16 = 11.6K\Omega$

Let C = 0.05 μF

$R = 1 / 2\ fC = 1/ (2 * 1 * 10^3 * 0.05 * 10^{-6}) =$

Circuit Diagram

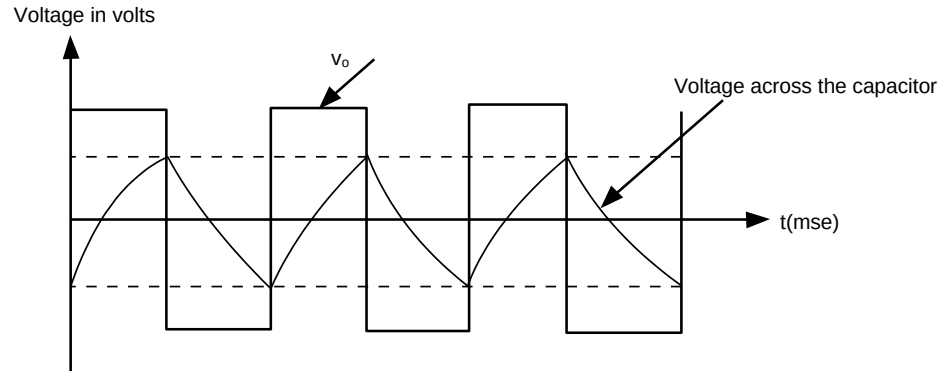


SYMMETRICAL ASTABLE MULTIVIBRATOR

Tabulation:

S.No			

Model graph



Procedure:

1. Make the connections as shown in the circuit diagram
2. Keep the CRO channel switch in ground and adjust the horizontal line on the x axis so that it coincides with the central line.
3. Select the suitable voltage sensitivity and time base on the CRO.
4. Check for the correct polarity of the supply voltage to op-amp and switch on power supply to the circuit.
5. Observe the waveform at the output and across the capacitor. Measure the frequency of oscillation and the amplitude. Compare with the designed value.
6. Plot the Waveform on the graph.

Design:

f = 1 KHz

T = 1/f = 1ms

$\beta = R_1 / (R_1+R_2)$

Let $R_1 = 10K\Omega$, and $R_2 = 10K\Omega$

Then $\beta = 0.5$

Therefore T= 2.2RC =1ms

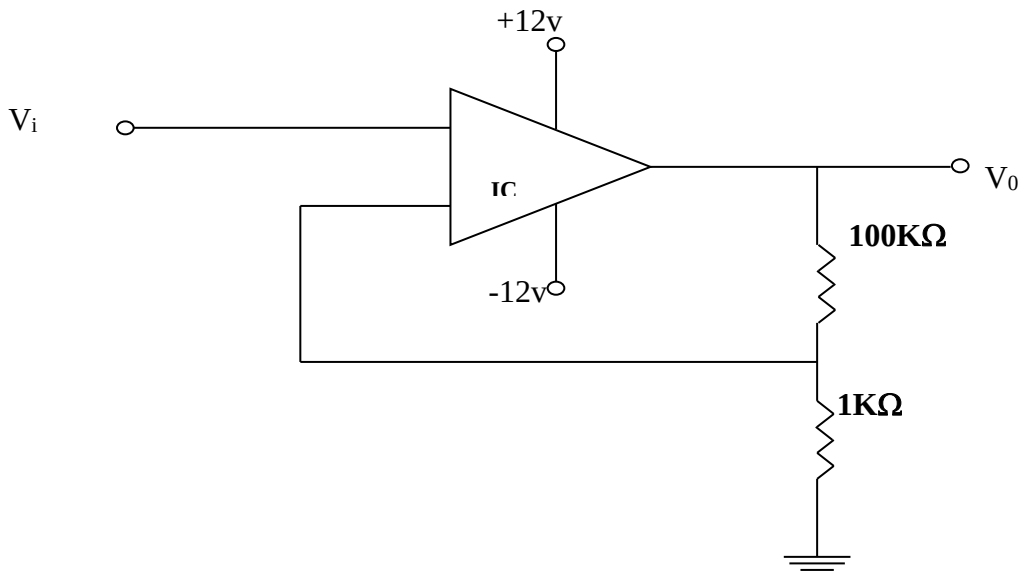
Schmitt Trigger:

Design

V_{CC} = 12 V; V_{SAT} = 0.9 V_{CC}; R1= 47KΩ; R2 = 120Ω

V_{UT} = + [V_{SAT} R_2] / [R_1+R_2] & V_{LT} = - [V_{SAT} R_2] / [R_1+R_2] & HYSTERSIS [H] = V_{UT} - V_{LT}

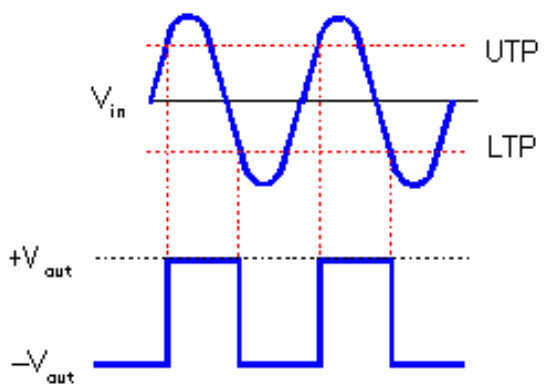
Circuit Diagram



Tabulation:

S.No			

Model Graph



Procedure

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than V_{cc})
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode and switch the trigger source in CRO to CHI.
5. Plot the input and output waveforms on the graph.

Result:

Thus Astable & Monostable Multivibrators and schmitt trigger were designed using op-amp and the waveforms were plotted.

6. RC PHASE SHIFT AND WIEN BRIDGE OSCILLATORS USING OP-AMP.

Aim:

To design the following sine wave oscillators

a) Wein Bridge Oscillator with the frequency of 1 KHz.
b) RC Phase shift oscillator with the frequency of 200 Hz.

Components Required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual trace supply	(0-30) V	1
3.	Function Generator	(0-2) MHz	1
4.	Resistors		
5.	Capacitors		
6	CRO	(0-30) MHz	1
7	Probes	--	--

Equations Related to the Experiments:

a) Wein Bridge Oscillator

Closed loop gain $A_v = (1+R_f/R_1) = 3$

Frequency of Oscillation $f_a = 1/(2\pi RC)$

b) RC Phase shift Oscillator:

Gain $A_v = [R_f/R_1] = 29$

Frequency of oscillation $f_a = 1\sqrt{6} * 2 * \pi * RC$

1) Wein Bridge Oscillator:

Design:

Gain required for sustained oscillation is $A_v = 1/\beta = 3$

(PASS BAND GAIN) (i.e.) $1+R_f/R_1 = 3$

$\therefore R_f = 2R_1$

Frequency of Oscillation $f_o = 1/2\pi\ R\ C$

Given $f_o = 1$ KHz

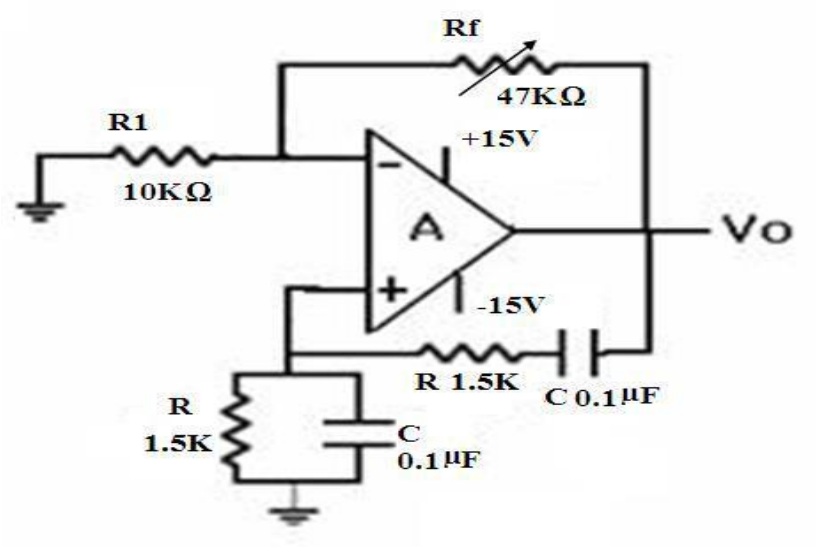
Let C = 0.05 μF

$\therefore R = 1/2\ \pi\ f_oC$

R = 3.2 KΩ

Let R1 = 10 KΩ $\quad\quad$ $\therefore$ Rf = 2 * 10 KΩ

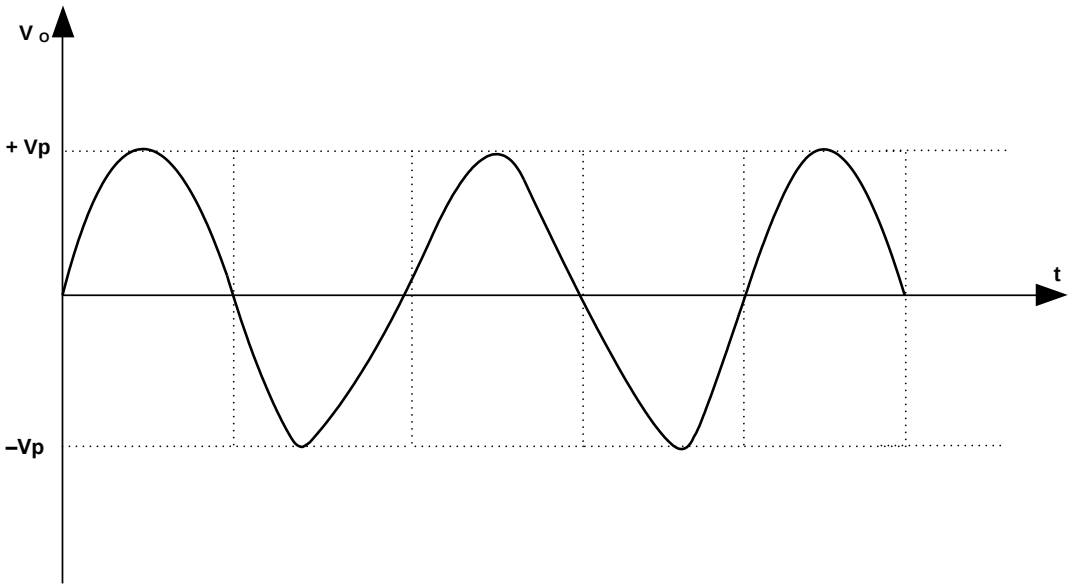
Circuit diagram:



Tabulation:

Derived frequency (Hz)	Observed frequency (Hz)	Amplitude (V)	Time period (ms)

Model Graph:



Procedure:

1. Connect the components as shown in the circuit

2. Switch on the power supply and CRO.
3. Note down the output voltage at CRO.
4. Plot the output waveform on the graph.
5. Redesign the circuit to generate the sine wave of frequency 2KHz.
6. Compare the output with the theoretical value of oscillation.

Observation:

Peak to peak amplitude of the output = Volts.
Frequency of oscillation = Hz.

2) RC Phase Shift Oscillators:

Design:

Frequency of oscillation fo = $1/(\sqrt{6}*2*\Pi*RC)$
Av = [Rf/R1] = 29
$R_1 = 10\ R$
$R_f = 29\ R_1$
Given fo = 200 Hz.
Let C = 0.1μF

$$R = 1/\left(\sqrt{6} * 2\,\pi * fo * C\right)$$

$$= 1/\left(\sqrt{6} * 2 * \pi * 200 * 0.1 * 10^{-6}\right)$$

= KΩ

To prevent the loading of amplifier by RC network, $R1 \geq 10R$

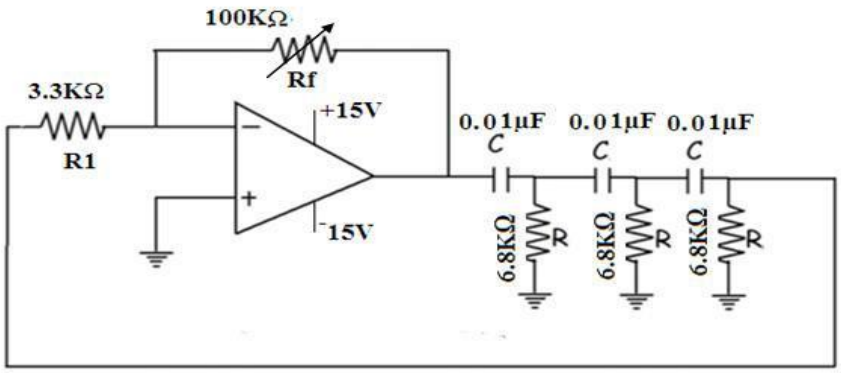
$\therefore R1 = 10 * ------$ = KΩ

Since $Rf = 29R1$

$Rf = 29 * ------$

= MΩ

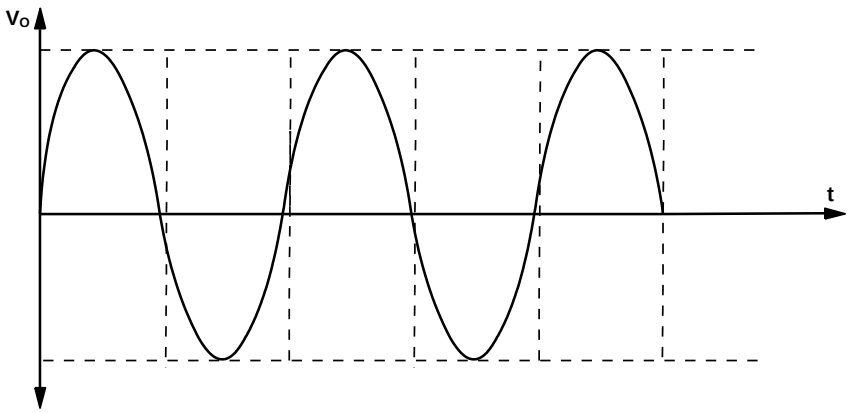
Circuit diagram:



Tabulation:

Derived frequency (Hz)	Observed frequency (Hz)	Amplitude (V)	Time period (ms)

Model Graph:



Procedure:

1. Connect the circuits as shown in the circuit 5.2
2. Switch on the power supply Note down the output voltage on the CRO.
3. Plot the output waveforms on the graph.
4. Redesign the circuit to generate the sine wave of 1 KHz.
5. Plot the output waveform on the graph.
6. Compare the practical value of the frequency with the theoretical value.

Observation:

Peak to peak amplitude of the sine wave = Volts

Frequency of Oscillation (obtained) = Hz.

Result:

Thus wien bridge oscillator and RC Phase shift oscillator was designed using op-amp and tested.

7. ASTABLE AND MONOSTABLE MULTIVIBRATORS USING NE555 TIMER.

Aim:

To design and test an Astable and Monostable Multivibrators using 555 timer with duty cycles ratio.

Apparatus Required:

S.No	Component	Range	Quantity
1.	555 TIMER		1
2.	Resistors	3.3K, 6.8k	1
3.	Capacitors	0.1 μ F, 0.01μ F	2
4.	Diode	In4001	1
5.	CRO		1
6.	Power supply	± 15 V	1
7.	Probe		2
8.	Bread Board		1

Astable Multivibrators using 555

Fig shows the 555 timer connected as an Astable Multivibrators. Initially, when the output is high. Capacitor C starts charging towards V_{cc} through R_A and R_B. As soon as capacitor voltage equals 2/3 V_{cc} upper comparator (UC) triggers the flip flop and the output switches low. Now capacitor C starts discharging through R_B and transistor Q_1.

When the voltage across C equals 1/3 V_{cc} lower comparator (LC), output triggers the flip-flop and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between 2/3 V_{cc} and 1/3 V_{cc} respectively. The time during which the capacitor charges form 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by

$$T_c = 0.69(R_A+R_B)C \qquad (1)$$

Where R_A and R_B are in Ohms and C is in farads. Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by

$$T_d = 0.69\ R_B\ C \qquad (2)$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69\ (R_A + 2R_B)\ C} \qquad (3)$$

The frequency of oscillation

$$f_o = 1 / T = 1.45 / (R_A + 2R_B)C \qquad (4)$$

Eqn (4) shows that fo is independent of supply voltage Vcc

The duty cycle is the ratio of the time t_d during which the output is low to the total time period T. This definition is applicable to 555 Astable Multivibrators only; conventionally the duty cycle ratio is defined as the ratio as the time during which the output is high to the total time period.

$$\therefore \text{ Duty cycle } = \frac{t_d}{T} \times 100$$

$$\frac{R_B}{R_A + 2R_B} \times 100 \qquad (5)$$

To obtain 50% duty cycle a diode should be connected across R_B and R_A must be a combination of a fixed resistor and a potentiometer. So that the potentiometer can be adjusted for the exact square waves

DESIGN:

Design an Astable Multivibrators for a frequency of _____KHz with a duty cycle ratio of D = 50 %

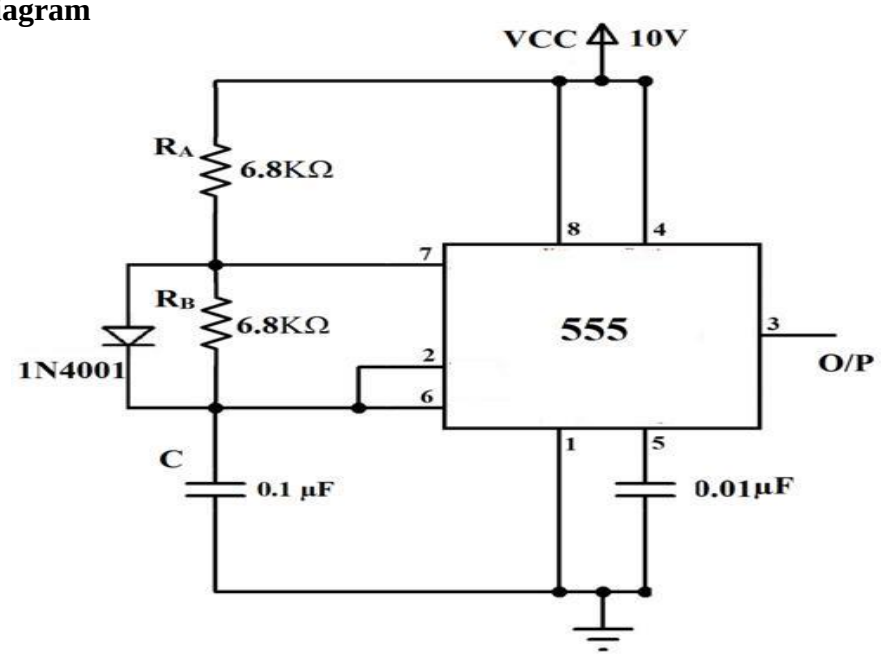
$fo = 1/T = 1.45 / (R_A+2R_B)C$

Choosing C = 1 μF; R_A = 560

$D = R_B / R_A + 2R_B = 0.5$ [50%]

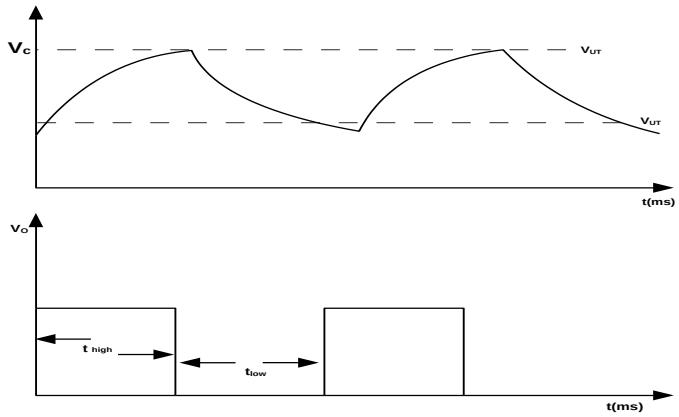
R_B = _____

Circuit Diagram



Tabulation:

Model Graph



Procedure:

1. Rig-up the circuit of 555 Astable Multivibrators as shown in fig with the designed value of components.
2. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
3. Switch on the power supply to CRO and the circuit.
4. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings and frequency.
5. Switch off the power supply. Connect a diode across R_B as shown in dashed lines in fig to make the Astable with 50 % duty cycle ratio. Switch on the power supply. Observe the output waveform. Draw to scale on a graph sheet.

Monostable Multivibrators using 555

Monostable Multivibrators has one stable state and other is a quasi stable state. The circuit is useful for generating single output pulse at adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components, resistor and a capacitor.

The stable state is the output low and quasi stable state is the output high. In the stable state transistor Q1 is ‘on’ and capacitor C is shorted out to ground. However upon application of

a negative trigger pulse to pin2, Q1 is turned 'off' which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{cc} through R_A. However when the voltage across C equal 2/3 V_{cc} the upper comparator output switches form low to high which in turn drives the output to its low state via the output of the flip flop. At the same time the output of the flip flop turns Q1 'on' and hence C rapidly discharges through the transistor. The output remains low until a trigger is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 Vcc. The width of the output pulse is given by,

$$T = 1.1\ R_A C$$

Design:

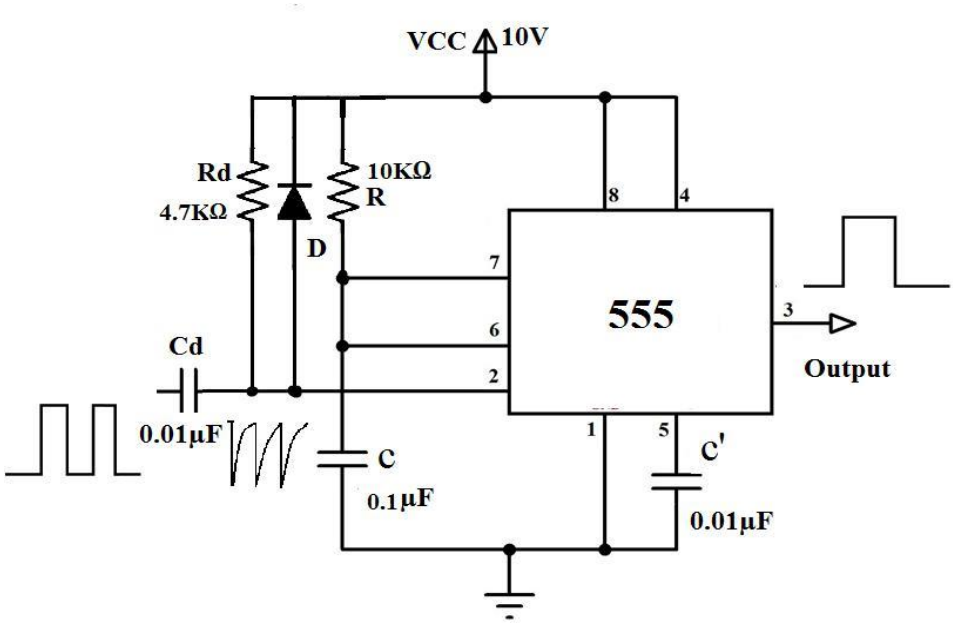
Given a pulse width of duration of 100 μs

Let C = 0.01 mfd; F = _____KHz

Here, $T = 1.1\ R_A C$

So, R_A =

Circuit Diagram:



Tabulation:

Model Diagram:

Procedure:

1. Rig-up the circuit of 555 monostable Multivibrators as shown in fig with the designed value of components.
2. Connect the trigger input to pin 2 of 555 timer form the function generator.
3. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
4. Switch on the power supply to CRO and the circuit.
5. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings along with trigger pulse.

Observation:

Peak to peak amplitude of the output = Volts.

Frequency = Hz.

Upper threshold voltage = Volts.

Lower threshold voltage = Volts.

Result:

Thus the Astable Multivibrators and Monostable Multivibrators using 555 timer is designed and tested.

9. DC POWER SUPPLY USING LM317 AND LM723.

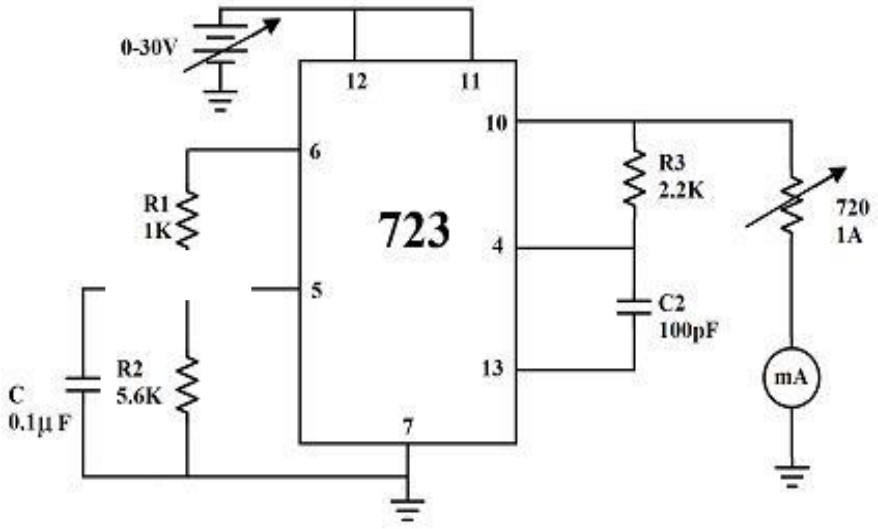
AIM :

To design a high current, low voltage and high voltage linear variable dc regulated power supply and test its line and load regulation.

COMPONENTS REQUIRED :

S.NO	COMPONENTS	SPECIFICATION	QUANTITY
1.	Transistors	TIP122,2N3055	1 each
2.	Integrated Circuit	LM723	1
3.	Digital Ammeter	(0 – 10) A	1
4.	Digital Voltmeter	(0 – 20) V	1
5.	Variable Power Supply	(0 – 30) V-2A	1
6.	Resistors	300Ω,430Ω,1KΩ,678KΩ,678Ω 1Ω	1 each 2
7.	Capacitors	0.1μF,100pF	1 each
9.	Rheostat	(0 – 350) Ω	1

CIRCUIT DIAGRAM: Low Voltage Regulator



DESIGN:

Output voltage → V_O

Reference voltage→ Vref

Rprotect → Minimum Resistance to protect the output from short circuit.

Low Voltage Regulator :

Given : Vo=5V, Vref = 7.15 V

To calculate R1, R2 ,R3 and Rsc.

Vo = Vref (R2 / (R1 + R2))

5 / 7.15 = (R2 / (R1 + R2))

(R1 + R2) 0.699= R2

0.699R1 = 0.301 R2 , R1 = 0.4306 R2

Select **R2 = 1 KΩ**

R1 = 1 KΩ * 0.4306 = 430Ω

R1 = 430Ω

R3 = R1 * R2 / (R1 + R2) , R3 = 430.6 *1000 /(430.6+1000)

R3 = 300Ω

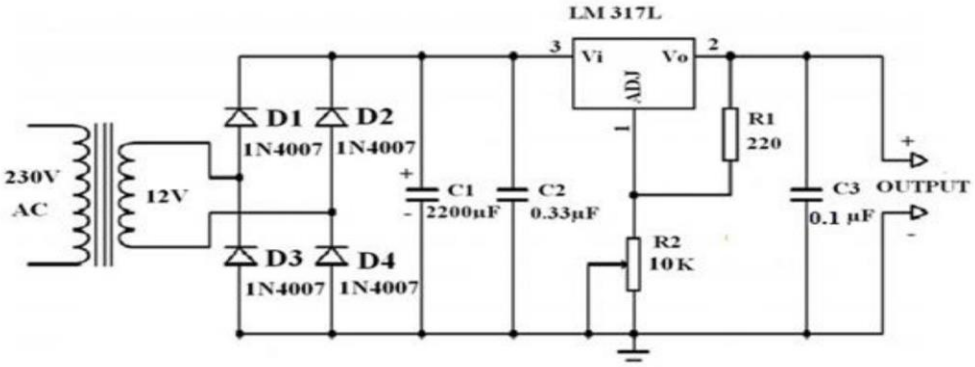
Rsc = V_{sense} / I_{limit} = 0.5 /1A = 0.5Ω , **Rsc = 0.5Ω**

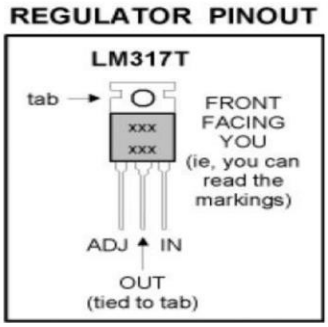
High Voltage Regulator :

Sl. No.	Name of item & specifications	Quantity
1	Multimeter	2
2	Resistor	1
3	Potentiometer	1
4	Capacitor	3
4	IC LM 317	1
5	Transformer (230 / 12 V)	1
7.	Diode 1N4001	4
8	Bread board	1
9	Connecting Wires	As required

CIRCUIT DIAGRAM:

High Voltage Regulator:





High Voltage Regulator :

<u>Given : Vo=12V, Vref = 7.15 V</u>

To calculate R1, R2 ,R3 and Rsc.

Vo = Vref (1 + (R1 / R2))

12 / 7.15 = 1+ (R1 / R2)

(12 / 7.15) - 1 = (R1 / R2)

(R1 / R2) = 0.678

Select **R2 = 1 KΩ**

R1 = 1 KΩ * 0.678 = 678Ω

R1= 678Ω

Rsc = V_{sense} / I_{limit} = 0.5 /1A = 0.5Ω

Rsc = 0.5Ω

Tabulation of the Measurements :

LOW VOLTAGE REGULATOR :

Line Regulation : **Load Regulation**

S.No.	Load Resistance R_{L1} =		Input Voltage V_{in1} =	
	Input Voltage Vin(Volts)	Output Voltage V_L(Volts)	Input Voltage Vin(Volts)	Output Voltage V_L (Volts)

HIGH VOLTAGE REGULATOR :

Line Regulation : **Load Regulation :**

S.No.	Load Resistance R_{L1} =		Input Voltage V_{in1} =	
	Input Voltage Vin(Volts)	Output Voltage V_L(Volts)	Input Voltage I_L (A)	Output Voltage V_L (Volts)

Calculation of % Voltage Regulation :

% Voltage Regulation = (V_{dc} (NL) - V_{dc} (FL)) / V_{dc} (FL)

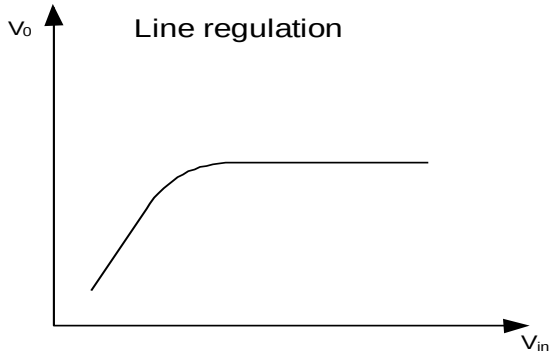
V_{dc} (NL) = D.C. output voltage on no load

V_{dc} (FL) = D.C. output voltage on full load

Model Graph :

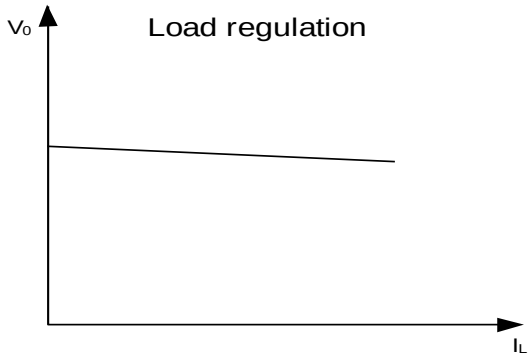
Line Regulation :

Input Voltage Vs Output Voltage :



Load Regulation :

Output Current Vs Output Voltage



PROCEDURE :

LOW VOLTAGE REGULATOR :

Line Regulation :

1. Give the circuit connection as per the circuit diagram shown in Fig 1.1.
2. Set the load Resistance to give load current of 0.25A.
3. Vary the input voltage from 7V to 18V and note down the corresponding output voltages.
4. Similarly set the load current (I_L) to 0.5A & 0.9A and make two more sets of measurements.

Load Regulation :

1. Set the input voltage to 10V.

2. Vary the load resistance in equal steps from 350Ω to 5Ω and note down the corresponding output voltage and load current.

3.Similarly set the input voltage (Vin) to 14V & 18V and make two more sets of measurements.

Lab Report :

1.Plot the line regulation by taking Input Voltage (Vin) along X-axis and Output Voltage (V_L) along Y-axis for various load currents.

2.Plot the load regulation by taking load current (I_L) along X-axis and Output Voltage (V_L) along Y-axis for various input voltages.

3.Calculate its % Voltage Regulation using the formula.

HIGH VOLTAGE REGULATOR :

Line Regulation :

1.Give the circuit connection as per the circuit diagram shown in Fig 1.2.

2.Set the load Resistance to give load current I_L of 0.25A.

3.Vary the input voltage from 7V to 18V and note down the corresponding output voltages.

4.Similarly set the load current (I_L) to 0.5A & 0.9A and make two more sets of measurements.

Load Regulation :

1. Set the input voltage to 10V.

2. Vary the load resistance in equal steps from 350Ω to 15Ω and note down the corresponding output voltage and load current.

3.Similarly set the input voltage (Vin) to 14V & 18V and make two more sets of measurements.

Lab Report :

1.Plot the line regulation by taking Input Voltage (Vin) along X-axis and Output Voltage (V_L) along Y-axis for various load currents.

2.Plot the load regulation by taking load current (I_L) along X-axis and Output Voltage (V_L) along Y-axis for various input voltages.

3.Calculate its % Voltage Regulation using the formula.

Result :

Thus the line and load regulation of a high current, low voltage and high voltage linear variable dc regulated power supply was designed and tested.

10-BIT R-2R DIGITAL TO ANALOG CONVERTER

Aim : To design 4 bit R-2R ladder DAC using Op-Amp for an output voltage of 5 V when the input is 10 (Binary 1010).

Apparatus :

Sl. No.	Particulars	Specification	Quantity
1.	IC	µA741	02
2.	Resistors	As per design	-
3.	Multimeter	-	01
4.	Base board + connecting wires	-	01 Set

Procedure :

1. Connections are made as shown in the circuit diagram.
2. Digital input data is given at D3, D2, D1, D0 and corresponding analog output voltage V_0 is measured.
3. Tabulate the readings & plot the graph between V_o on y-axis V_{in} on X-axis.

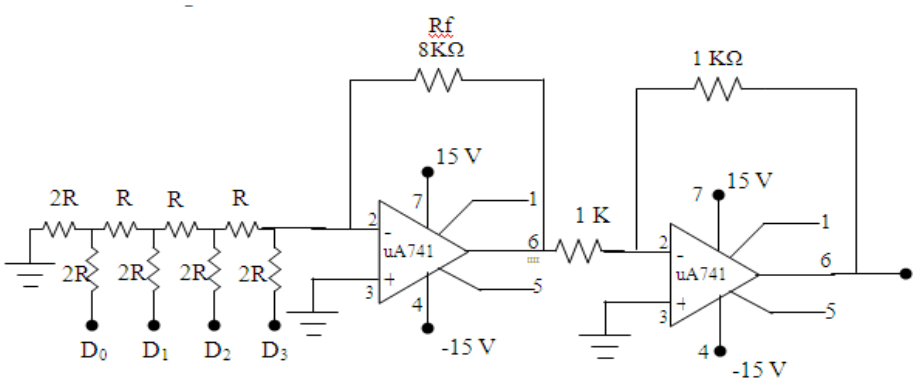
Note :

1. D0.D1.D2 & D3 are binary input.
2. Vo is the analog output.
3. Binary inputs Do.D1.D2 & D3 can take either the value '0' or '1'.
4. Binary input Di (i = 0 to 3) can be made '0' by connecting the i/p to ground. It can be made '1' by connecting to –5 V.

Logic 0 → 0V

Logic 1 → +5V

Circuit Diagram



Result :

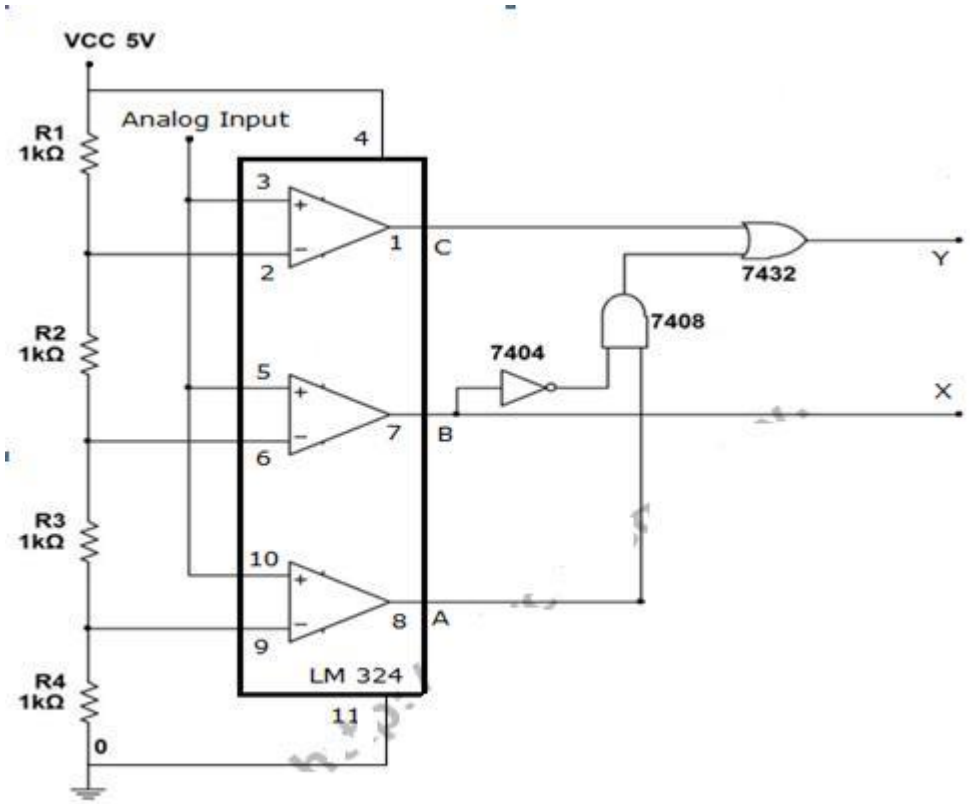
Decimal Value	Binary Inputs				Analog O/P Vo(volts) Theoretical values	Analog O/P Vo(volts) Practical values
	D_3	D_2	D_1	D_0		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

TWO BIT FLASH ADC

Aim : To realize two bit Flash ADC
Apparatus :

Sl. No.	Particulars	Specification	Quantity
1.	IC	LM324 7404 7432 7409	04
2.	Resistors	1K	04
3.	Multimeter	-	01
4.	Base board + connecting wires	-	01 Set

Circuit diagram



Procedure :

1. Connections are made as shown in the circuit diagram.
2. Apply the different analog input voltages and note down the output.

Tabulation and Result

Analog Input	A	B	C	Digital Output	
				X	Y
0 to $\frac{1}{4}Vcc$	0	0	0	0	0
$\frac{1}{4}Vcc$ to $\frac{2}{4}Vcc$	0	0	1	0	1
$\frac{2}{4}Vcc$ to $\frac{3}{4}Vcc$	0	1	1	1	0
$\frac{3}{4}Vcc$ to Vcc	1	1	1	1	1

10. STUDY OF SMPS.

Aim:

To study the switched-mode power supply.

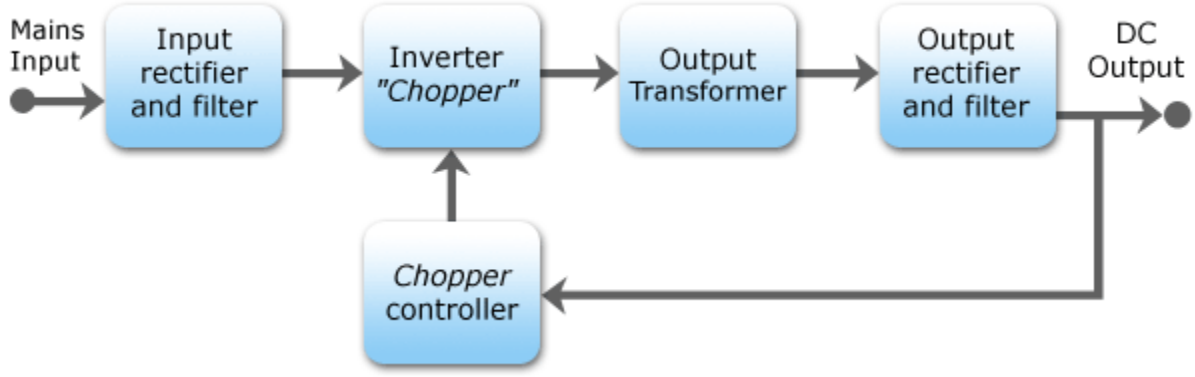
Apparatus required:

switched-mode power supply.

Block Diagram:

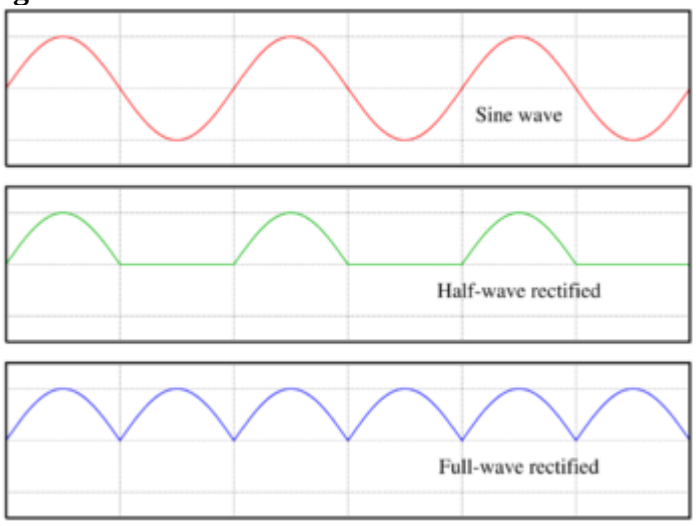
A switched-mode power supply (switching-mode power supply/SMPS, or simply switcher) is an electronic power supply unit (PSU) that incorporates a switching regulator in order to provide the required output voltage. An SMPS is a power converter that transmits power from a source (e.g., a battery or the electrical power grid) to a load (e.g., a personal computer). The function of the converter is to provide a regulated output voltage usually at a different level from the input voltage.

Block Diagram:



Block diagram of a mains operated AC–DC SMPS with output voltage regulation

Input rectifier stage



AC, half-wave and full-wave rectified signals.

If the SMPS has an AC input, then the first stage is to convert the input to DC. This is called rectification. The rectifier circuit can be configured as a voltage doubler by the addition of a switch operated either manually or automatically. This is a feature of larger supplies to permit operation from nominally 120 V or 240 V supplies. The rectifier produces an unregulated DC voltage which is then sent to a large filter capacitor. The current drawn from the mains supply by this rectifier circuit occurs in short pulses around the AC voltage peaks.

Inverter stage

The inverter stage converts DC, whether directly from the input or from the rectifier stage described above, to AC by running it through a power oscillator, whose output transformer is very small with few windings at a frequency of tens or hundreds of kilohertz (kHz). The frequency is usually chosen to be above 20 kHz, to make it inaudible to humans. The output voltage is optically coupled to the input and thus very tightly controlled.

Voltage converter and output rectifier

If the output is required to be isolated from the input, as is usually the case in mains power supplies, the inverted AC is used to drive the primary winding of a high-frequency transformer. This converts the voltage up or down to the required output level on its secondary winding. The output transformer in the block diagram serves this purpose.

Result:

Thus the switched-mode power supply was studied.

11. SIMULATION OF EXPERIMENTS 3, 4, 5, 6 AND 7 USING PSPICE NETLISTS.

Aim:

To simulate the following experiments using Pspice Netlist software.

1. Instrumentation amplifier.
2. Active Lowpass, Highpass and Bandpass filters.
3. Astable and Monostable multivibrators and Schmitt trigger using Op-Amp.
4. Phase shift and Wien bridge oscillators using Op-Amp.

Apparatus Required:

Personal computer workstation available in the laboratory. PSpice circuit simulator and Probe graphic post processor software available on the PC.

Theory:

PSPICE (Simulation Program with Integrated Circuit Emphasis).is a general purpose circuit simulation programming language that performs non-linear DC, transient and linear steady state AC analysis. Linear circuit elements of resistance, capacitance, inductance, independent and dependent current and voltage sources are modeled. Personal

- To start PSpice, double click on the PSpice schematic icon or select schematic from the design eval software menu:
- Draw schematics:
    1. Select the desired component from DRAW/GET NEW PART and place the part.
    2. Repeat the first step until all necessary parts are placed.
    3. Connect each component with the DRAW/WIRE command.
    4. Save the Circuit with your initials in your directory.
    5. Select desired analysis and set the options (ANALYSIS/SETUP)
    6. Run PSpice (ANALYSIS/RUN PSPICE)
- If errors are found, they will be described in the *my_file*.OUT file after execution. View the contents of this file using ANALYSIS/EXAMINE OUTPUT.

- During this experiment, hard copy output will not be required.

PROCEDURE:

1. For each circuit perform the following:
    - Draw the circuit scematic in Pspice, label all the nodes.
    - Setup the analysis for a DC sweep from -5V to 5V in 0.1V increments.
    - Run the simulation. Display the correct I-V graph in Probe.
    4. Record the annotated circuit diagram, the simulation results, graphs and your comments in your laboratory notebook. Have your instructor inspect

Result:

The experiments were simulated using Pspice and the results were Compared.